V-Band GaAs MMIC Low-Noise and Power Amplifiers

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Abstract—**GaAs monolithic amplifiers based on MESFET technology have been developed at V-band for low-noise and power applications. These MMIC's, which have on-chip dc-blocking and bias networks, were fabricated from both VPE and MBE materials and then evaluated. The low-noise designs resulted in a single-stage MMIC LNA achieving a 6.5 dB noise figure and a 4.1 dB gain at 59 GHz, as well as a cascaded six-stage amplifier exhibiting an 8 dB minimum noise figure and a 30 dB gain from 56.2 to 60 GHz. The single-stage power amplifier provided over 4.5 dB of gain from 57 to 60.5 GHz, with a maximum output power of 95 mW and a corresponding power-added efficiency of 11 percent at 58 GHz. Maximum power-added efficiency of 15.3 percent at 73 mW was also obtained. A cascaded four-stage amplifier demonstrated stable operation, achieving 17 dB of gain and 85 mW of output power. In addition, a two-stage balanced amplifier provided 136 mW of output power and 7.5 dB of linear gain from 56.5 to 61.5 GHz. These results demonstrate that excellent low-noise performance and power/gain performance are achievable with MESFET MMIC's, in the 60 GHz band.**

I. Introduction

MILLIMETER-WAVE field-effect transistor (FET) devices and circuits such as low-noise amplifiers (LNA's) and power amplifiers (PA's) are currently being developed for potential applications in intersatellite link, phased-array, spaceborne radar, and electronic warfare systems. Discrete modulation-doped FET's (MODFET's) have shown excellent device noise performance of 2.6 dB and associated gain of 5.7 dB at 62 GHz, as well as device power results of 50 mW of output power, 3 dB of gain, and 11 percent efficiency at V-band [1]. InGaAs/GaAs pseudomorphic MODFET's have also demonstrated similar noise measure [1] and device output power of 20 mW at 60 GHz [2]. More recently, a discrete GaAs metal semiconductor FET (MESFET) with a pulse-doped InGaAs channel showed an output power of 40 mW, with a power-added efficiency of 14 percent at 60 GHz [3].

In the monolithic microwave integrated circuit (MMIC) area, a 30 GHz MESFET LNA with a 7 dB noise figure and 14 dB of gain was presented [4]. Recently, a single-stage monolithic MODFET LNA was reported at 44 GHz [5], while a V-band power MMIC with a 100 μm gate width MESFET has demonstrated 25 mW of output power with 8 percent efficiency at 54 GHz [6]. Because no input and output dc-blocking elements were included in these designs, and because bias networks were also omitted in some cases, direct cascading of the MMIC's to achieve usable gain was not possible.

This paper presents new data and better performance results than those recently reported [7], [8] regarding the use of MESFET's in LNA's and PA's for the 60 GHz band. A device/circuit computer-aided design (CAD) program developed at COMSAT Laboratories permitted parametric study of circuit performance with variation of the device structure and material parameters prior to MMIC fabrication. Single- and dual-stage LNA modules were developed from an optimized low-noise MESFET and a source-pull computer subroutine. For the power MMIC, an optimized device structure, together with a CAD load-pull subroutine developed in-house, allowed the successful use of MESFET's having larger gate widths than those previously reported to achieve high-output-power monolithic circuits.

In both types of circuits, built-in dc-blocking capacitors and bias networks have allowed cascading of the MMIC's. Usable power gain and stable operation have also been obtained with monolithic circuits from the initial design, without iteration. The millimeter-wave results demonstrated the application of MESFET's to MMIC LNA's and PA's, with excellent noise performance and highest gain/power achievement at V-band.

The following sections present the custom device designs, MMIC design approaches, fabrication process, and measured results. In general, a description common to both low-noise and power applications is presented, followed by a more detailed description of each device.

II. Device Designs

A device structure was first established by evaluating the performance of a bias-dependent equivalent circuit model and the dc characteristics of the low-noise and power MESFET's. The model was generated by a device-modeling computer program [9] based on device physics [10]–[12], MESFET geometrical dimensions, and material parameters. The program also includes subroutines that allow source-pull and load-pull studies of the device for the two applications.

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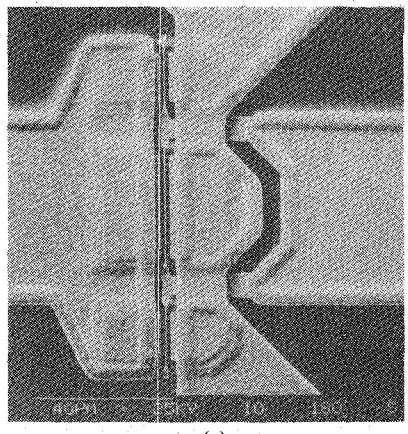
The above analysis, combined with commercially available CAD circuit programs, enable device/circuit performance to be studied parametrically by changing device parameters such as channel doping and thickness, gate length, and source-to-drain spacing. Thus, the MESFET can be optimized to provide the desired noise figure or output power and power-added efficiency for a given frequency band. Since the device structure and parameters have different requirements for the low-noise and power applications, material and processing parameters such as active channel thickness, gate-recess contour, maximum drain current, and pinch-off voltage were optimized differently. However, both types of MESFET's had nominal gate lengths of 0.3 μm and high doping densities (5×10^{17} cm^{-3}) for the active region. The gates were also offset toward the source.

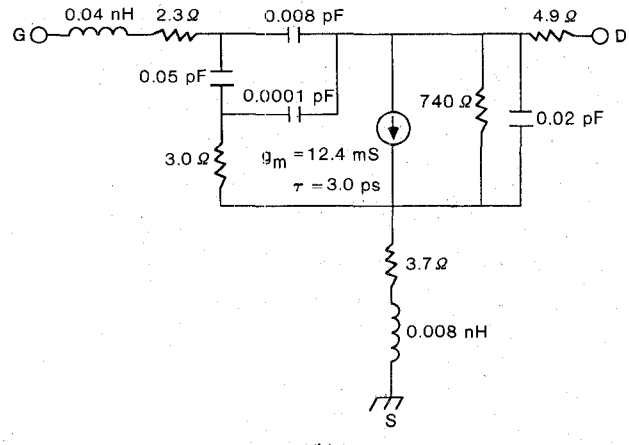
A. Low-Noise MESFET

The low-noise device used in the present study (Fig. 1(a)) had a total gate width of 60 μm and a dual-fed gate structure. An optimized gate length to channel height ratio, L_g/H_c, of 3 to 4 was used. The gate was recessed to achieve a low pinch-off of about 1 V. Fig. 1(b) shows the equivalent circuit of the MESFET at low noise bias. The corresponding calculated maximum frequency of oscillation is 105 GHz. The transconductance, g_m, increased to 16 mS at I_{dss}.

The noise parameters at *V*-band were estimated from noise modeling based on equivalent circuit element values generated by the device model, and on Fukui's empirical expressions for noise figure, noise resistance, and optimum source impedance [10], [11]. Devices processed using similar fabrication steps and geometry were characterized for noise parameters at a number of lower frequencies (below 18 GHz) to determine the "fitting factors" in the equations. The calculated parasitic resistances, R_g and R_s (corresponding to gate and source resistance, respectively), the intrinsic resistance, R_i, the transconductance, and the gate-to-source capacitance were used to calculate the noise parameters at *V*-band. The predicted complex conjugate of the optimum source impedance at 60 GHz, as shown in Fig. 2, was determined to be in the vicinity of the expected location on the Smith chart with respect to the input S_{11} of the extrapolated and calculated *S* parameters. Thus, the different approaches resulted in a consistent estimate of the noise parameters at 60 GHz.



(a)



(b)

Fig. 1. Low-noise MESFET from the *V*-band. MMIC. (a) Scanning electron micrograph. (b) Equivalent circuit model.

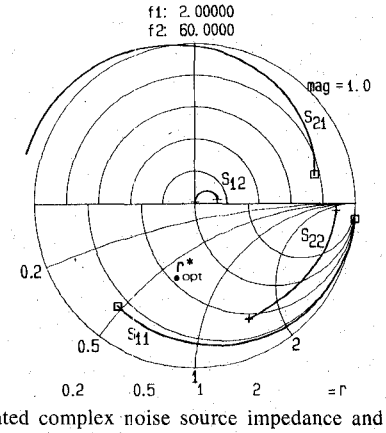
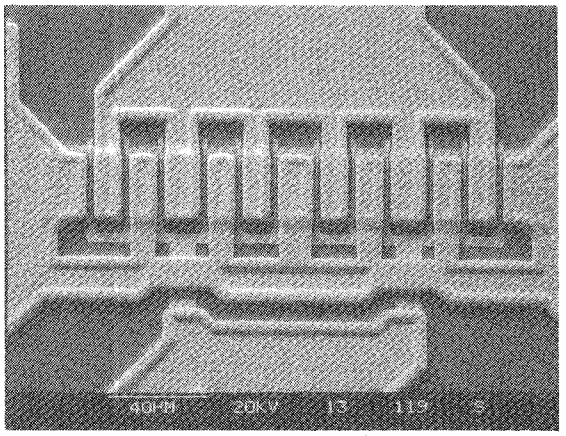


Fig. 2. Calculated complex noise source impedance and *S*-parameter of the low-noise MESFET.

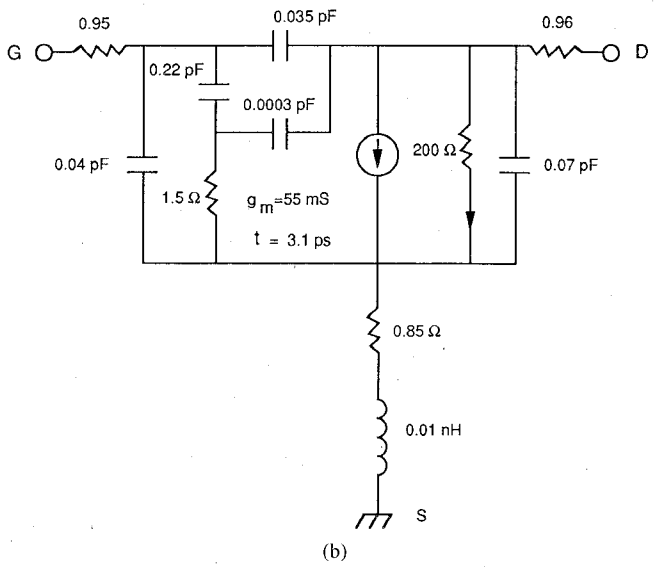
B. Power MESFET

Power device design and optimization were also performed using computer device modeling and the load-pull subroutine. The MESFET (Fig. 3(a)) consists of 12 gate fingers, with a unit gate width of 25 μm, for a total gate width of 0.3 mm. The sub-half-micron gate was recessed down to an appropriate channel height to achieve a pinch-off voltage of 2 V. This gate recess reduces source resistance, resulting in increased terminal transconductance, while proper recess shape allows high breakdown voltage (12–13 V) to be achieved. Fig. 3(b) shows the equivalent circuit model of the power MESFET. The calculated maximum frequency of oscillation is 89 GHz. It should be noted that the maximum available gain (*MAG*) of the device increases with source inductance at 60 GHz, but at the expense of stability. The measured dc transconductance was 50 to 60 mS for devices from different wafers, which corresponds to 167 to 200 mS/mm.

The two quantities calculated by the computer subrou-



(a)



(b)

Fig. 3. Power MESFET from the *V*-band MMIC. (a) Scanning electron micrograph. (b) Equivalent circuit model.

tine that are related to determining the MESFET output power capability are the knee voltage, V_k, and the maximum drain current, I_{max}. V_k is the drain voltage at the onset of drain current saturation, and I_{max} is the drain current when the gate is slightly forward biased (as is the case in large-signal operation). The subroutine then uses the bias-dependent equivalent circuit and the values of breakdown voltage (V_{bd}), V_k, and I_{max} to calculate the MESFET output power, linear gain, and power-added efficiency. This is accomplished by solving the node-voltage equations of the MESFET equivalent circuit with the following two constraints: the voltage between the drain and gate cannot exceed V_{bd} minus V_k, and the drain current cannot exceed I_{max}. After the node voltages are obtained, the input and output powers are calculated, for a given load impedance assigned at the output.

A built-in optimization routine varies the load impedance of the MESFET and solves the voltage and the current at each node of the equivalent circuit for each given load until a load impedance is found that maximizes the output linear power. The load can also be optimized for maximum power-added efficiency or maximum power

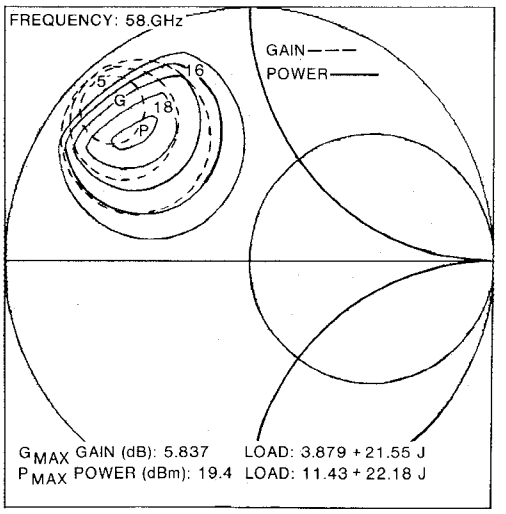


Fig. 4. Impedance contours for constant gain and constant output power of the 0.3 mm MESFET at 58 GHz.

gain. It was found that, as frequency increases, channel doping should increase while channel height should decrease. The gate length to channel height ratio should be kept above unity to maintain low output conductance of the MESFET.

Fig. 4 shows a sample of theoretically generated contours of constant gain and output power on the output impedance Smith chart for the designed 0.3 mm gate width MESFET. The maximum linear output power of the MESFET was calculated to be 87 mW when matched to the load of $11.4 + j22.2\ \Omega$, with an associated gain of 5 dB (*MAG* of 5.8 dB) at 58 GHz. These results were obtained by using I_{max} of 0.1 A, V_k of 1 V, and $V_{pinch\text{-}off}$ of 2 V, as derived from the device modeling program and an assumed V_{bd} of 12 V.

III. MMIC Designs

In designing the low-noise and power amplifiers for the present frequency band, distributed-element matching (as opposed to lumped-element matching) was employed to achieve low circuit loss and better modeling accuracy. The use of narrow, high-impedance transmission lines was avoided in order to minimize ohmic loss of the matching circuit, especially in the input circuit of the LNA and the output circuit of the PA. Shunt inductances were implemented as stubs shorted to ground through metal–insulator–metal (MIM) capacitors and via holes, while shunt capacitances were implemented as open-circuit elements.

A transmission line model of the input and output dc-blocking capacitors was used to account for their distributive characteristics. Input and output biases were provided by shunt RF-shorted elements, which were also grounded through MIM capacitors and via holes. The through-substrate via holes provided low-inductance grounding for the shorted shunt elements as well as the MESFET sources. The monolithic MIM capacitor model and the parasitic inductance associated with via holes were included in the circuit analysis.

In the LNA design, the input circuit of the single-stage

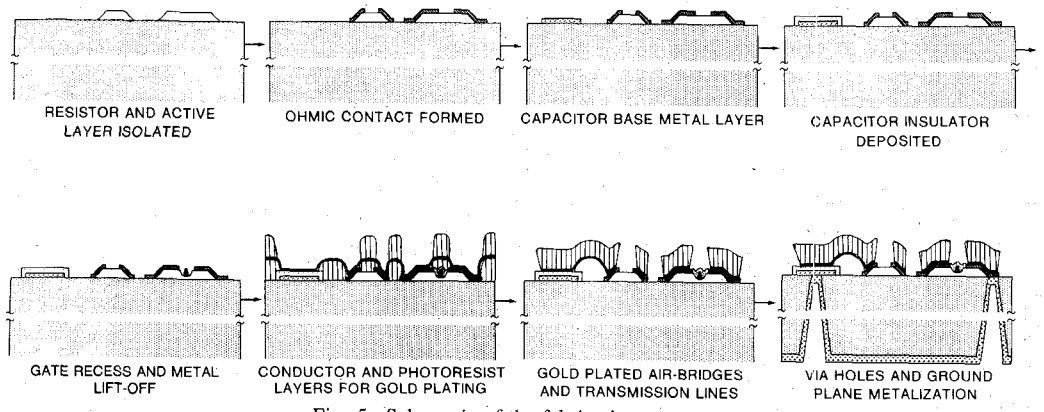


Fig. 5. Schematic of the fabrication processes.

amplifier was designed to match the optimal source impedance of the MESFET, resulting in low-noise performance. The output circuit, which included RF-shorted and open shunt elements, was then optimized for output return loss and gain flatness across the desired frequency band. In the two-stage design, the interstage matching network was used to optimize the bandwidth and the gain flatness of the amplifier. The output network of the second stage was optimized for the output return loss, in order to minimize impedance mismatch between the stages when MMIC modules were cascaded.

In the PA design, the output matching circuit presented the optimum load to the MESFET, resulting in maximum output power. The input matching circuit was designed to present a conjugate match to the input impedance of the MESFET, which was loaded with the optimal impedance. Since the input circuit was designed and optimized for return loss and gain response, with the series MIM dc-blocking capacitors (2 pF) integrated in the circuit, the amplifiers could be directly cascaded with good gain flatness across the frequency band.

At millimeter-wave frequencies, some uncertainty exists regarding the accuracy of commercially available circuit analysis programs, as well as the means of predicting associated device and circuit parasitics. A design approach was established that allowed slight adjustment of the matching circuits in subsequent fabrication runs after a preliminary circuit evaluation. "Tuning islands" were incorporated into the circuit layout which could then be connected via the direct e-beam write and gate metallization process. In addition, by carefully planning the amplifier layout during mask design, the same e-beam direct write scheme allowed different stages of MMIC's to be connected. Thus, multistage and/or balanced amplifiers on a single chip of larger size providing higher gain and/or power can be obtained.

These design approaches were applied to the LNA and PA MMIC's, enabling the designed performance to be achieved without additional mask iterations.

IV. MMIC Fabrication

COMSAT's baseline mesa MMIC process (similar to that previously reported for lower frequency MMIC's [13], [14], with sequence variation) was used to fabricate the monolithic amplifiers. Photolithography techniques, with e-beam direct write for the gate structures, were employed.

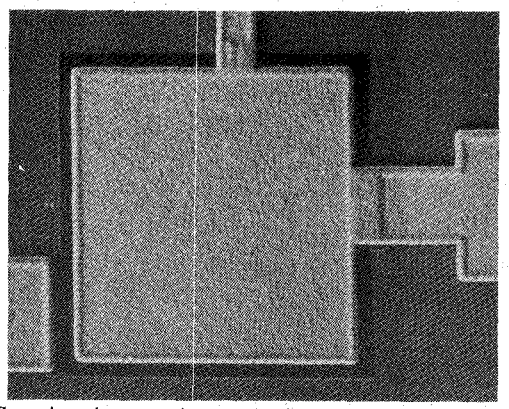


Fig. 6. Scanning electron micrograph of a capacitor including air/dielectric bridges.

Two types of GaAs materials were used for the present study. Layers of n^+-n-buffer structure were grown on Bridgman semi-insulating material by vapor-phase epitaxy (VPE). Also, n^+-n-p^- layers of GaAs were deposited by molecular beam epitaxy (MBE) onto undoped semi-insulating substrate grown by the liquid-encapsulated Czochralski (LEC) technique. In general, the MBE material provided a narrower transition region between the different layers and a more uniform doping density across the wafer than the VPE material.

Fig. 5 is a schematic of the major processing steps. The fabrication process began with mesa isolation for the active devices and resistors. A rapid-thermal annealed Au/Ge/Ni/Ag/Au alloy was used for the ohmic contact, and MIM capacitor base metal was defined by lifting off Ti/Pt/Au. The 2500-Å-thick Si_3N_4 dielectric for the MIM capacitor (Fig. 6) was deposited by plasma-enhanced chemical vapor deposition (PECVD).

An evaporated Ti/Pt/Au metallization was employed for the gates. Fig. 7 shows the detailed gate structure of the LNA MESFET. The air bridge structures and transmission lines were fabricated using two mask levels: plating-via and plating. The top plate metallization was Ti/Au

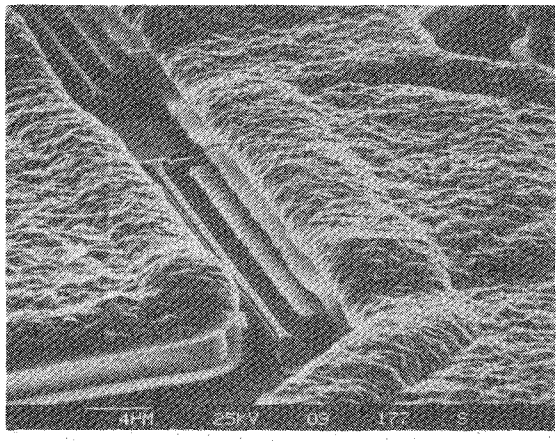


Fig. 7. Scanning electron micrograph of the low-noise MESFET gate region.

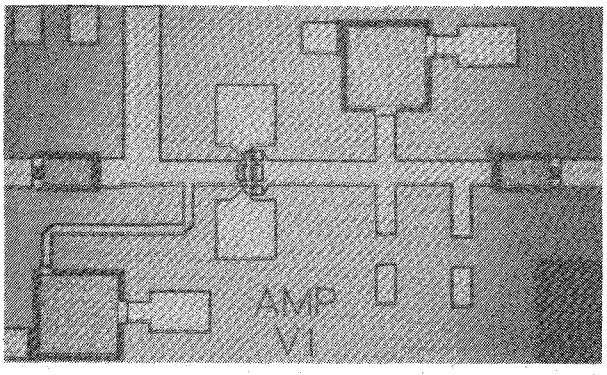


Fig. 8. *V*-band single-stage MMIC LNA.

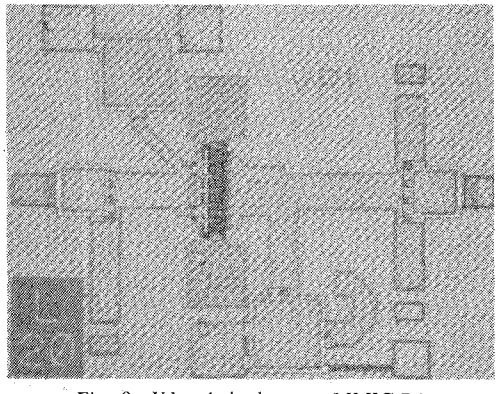


Fig. 9. *V*-band single-stage MMIC PA.

at a thickness of 2 μm. Through-substrate via holes were attained by infrared and spray etch techniques. The via hole size is nominally 50 μm^2.

The area sizes of the 0.08-mm-thick chips for the single- and dual-stage LNA MMIC's are 1.6 mm × 0.75 mm and 2 mm × 0.75 mm, respectively. The size of the single-stage PA MMIC is 1.0 mm × 0.75 mm × 0.08 mm. Figs. 8 and 9 show samples of a single-stage LNA and PA, respectively.

V. Measured Results

To accurately measure the performance of the MMIC's, test fixtures for amplifier evaluation were first developed, and the calibrations of the measurement systems were validated. These procedures are described in this section, together with the measured performance of the low-noise and power amplifiers.

A. Amplifier Housing and Measurement Calibration

V-band waveguide-to-microstrip transitions with low RF loss were fabricated using finline structures on 0.127-mm-thick fused-silica substrates. The finline patterns, which were printed on both sides of the substrate, consisted of two antipodal exponential tapers that transform the impedance of the WR-15 waveguide into the 50 Ω impedance of the microstrip line. The *E* field of the empty waveguide is rotated 90° as it passes through the tapers to a balun, which also prevents reflection of unbalanced modes from the microstrip section inside the waveguide. Serrations were printed on the substrate to act as a millimeter-wave frequency choke at the gap between the two halves of the waveguide. This arrangement avoided the necessity of making mechanical contact between the upper waveguide half and the side edges of the substrate in order to achieve RF-short conditions at those locations.

Fig. 10 depicts a sample of the amplifier assembly, with two waveguide-to-microstrip transitions and a single-stage MMIC LNA on the center block. The performance of two waveguide-to-microstrip transitions and two lengths of 1.9-mm-long fused-silica substrate measured back-to-back is shown in Fig. 11. The insertion loss and the return loss of one waveguide-to-microstrip transition were 0.5–0.7 dB and better than 18 dB, respectively, from 50 to 63 GHz.

The MMIC's were mounted on a copper test fixture, which included bias feedthroughs and a short 50 Ω microstrip line at the input and the output of the monolithic circuits for ease of assembly and disassembly. The length of each line was 1.5 to 2.5 mm, depending on the size and number of cascaded MMIC's, and its RF loss was included in the measured results. This versatile evaluation approach permitted modules to be cascaded in a multistage amplifier configuration. Furthermore, coaxial launchers could be used with the center-block test fixture. Investigation of the MMIC's at lower frequencies for any spurious signal was performed using this configuration.

Special attention was given to evaluation methods and calibration techniques for the MMIC's at the millimeter-wave frequencies of interest. The Hewlett-Packard (HP) 40–60 GHz measurement system was used to obtain the fabricated MMIC frequency responses. This was supplemented by a Hughes IMPATT source to measure both gain response and power performance at higher frequencies. The accuracy of the swept responses was verified by measuring sampled amplifiers using a Hughes *V*-band network analyzer at the Rome Air Development Center (RADC), Hanscom Air Force Base, Massachusetts. Fig. 12(a) shows a comparison of the gain response measurements of a multistage amplifier.

The noise figure was measured using the hot and cold load technique, with a mixer and an HP noise figure meter. The typical *Y* factor for a dual-stage LNA is 0.25 to

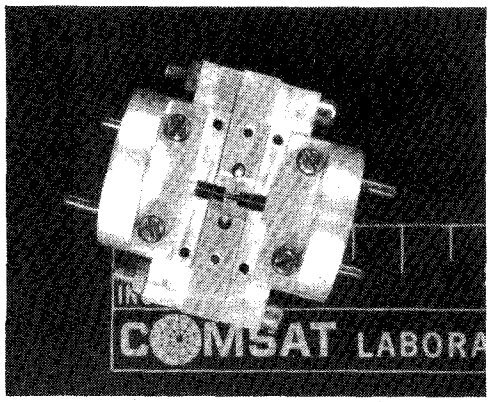


Fig. 10. Sample amplifier assembly with waveguide-to-microstrip transitions and a single-stage MMIC LNA on the center block.

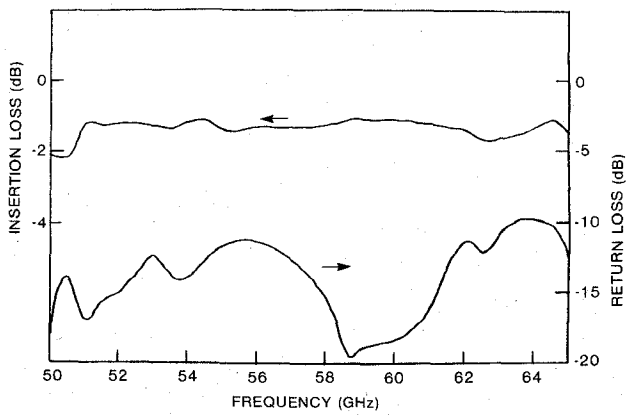


Fig. 11. Performance of two antipodal finline waveguide-to-microstrip transitions.

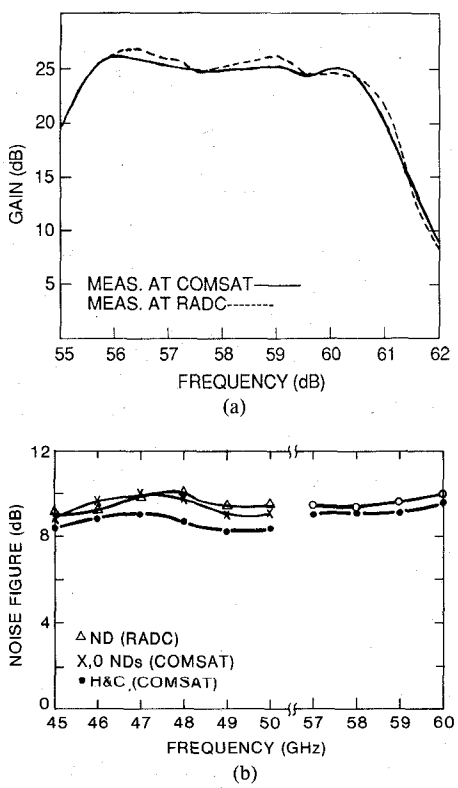


Fig. 12. Comparison of gain response and noise measurements from different sources. (a) Gain response of multistage amplifier. (b) Noise figure of measurement system.

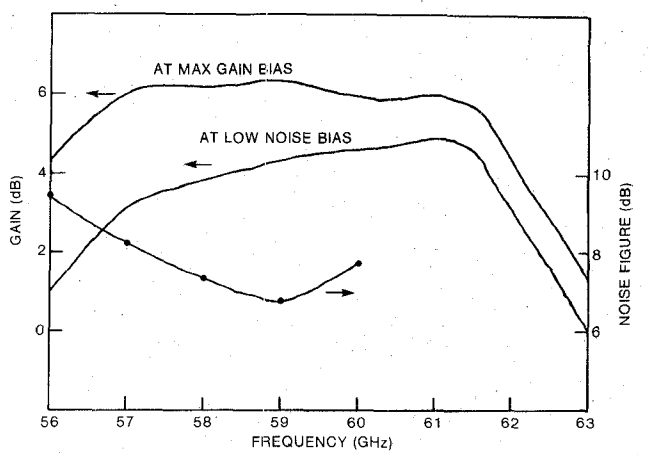


Fig. 13. Noise figure and gain versus frequency of a single-stage MMIC LNA.

0.3 dB. The calibration of the measurement technique was compared with two other commercially available noise diodes (one from RADC) up to their maximum operating frequency of 50 GHz (Fig. 12(b)). More recently, the results of the hot and cold load technique were compared with those for a new commercial noise diode operating to 60 GHz, and were found to be within 0.3 dB.

Power was measured using factory-calibrated HP detectors and Hughes power sensors. At 58 GHz, there was a 0.03 dB difference in measured power between the two methods. An HP spectrum analyzer was used to monitor the level of spurious signals during the power measurements. Any observable spurious signal was identified to be from the IMPATT source and was reduced through filtering to at least 25 dB below the carrier.

B. Low-Noise MMIC Amplifier Results

Single-stage and two-stage MMIC LNA's from both VPE and MBE wafers were evaluated. Fig. 13 shows the measured performance of a single-stage LNA from a VPE wafer. A small-signal gain of 3.2 to 4.8 dB was obtained from 57 to 61.5 GHz. A noise figure of 6.5 dB, and an associated gain of 4.1 dB, were achieved at 59 GHz. The nominal bias parameters of the devices are a drain voltage of 3.5 V and a drain current of 7 to 10 mA. At higher drain current bias, a power gain of 6 dB was obtained for a bandwidth of 4.5 GHz. Noise figure was not measured above 60 GHz because the available IMPATT source was found to be excessively noisy.

Fig. 14 depicts the results for the dual-stage MMIC amplifier from a VPE wafer. Linear gain of better than 7 dB and a minimum noise figure of 7.8 dB were obtained in the frequency range of 56 to 62 GHz. The modules could provide more than 10 dB gain at a higher drain current bias. Nominal output power was better than 12 dBm. Fig. 15 shows the output versus input power of a dual-stage amplifier. A power density of 0.27 W/mm has been achieved at 1 dB gain compression.

The performance of the single- and dual-stage MMIC's from recent MBE wafer runs is shown in Fig. 16. A 2 dB

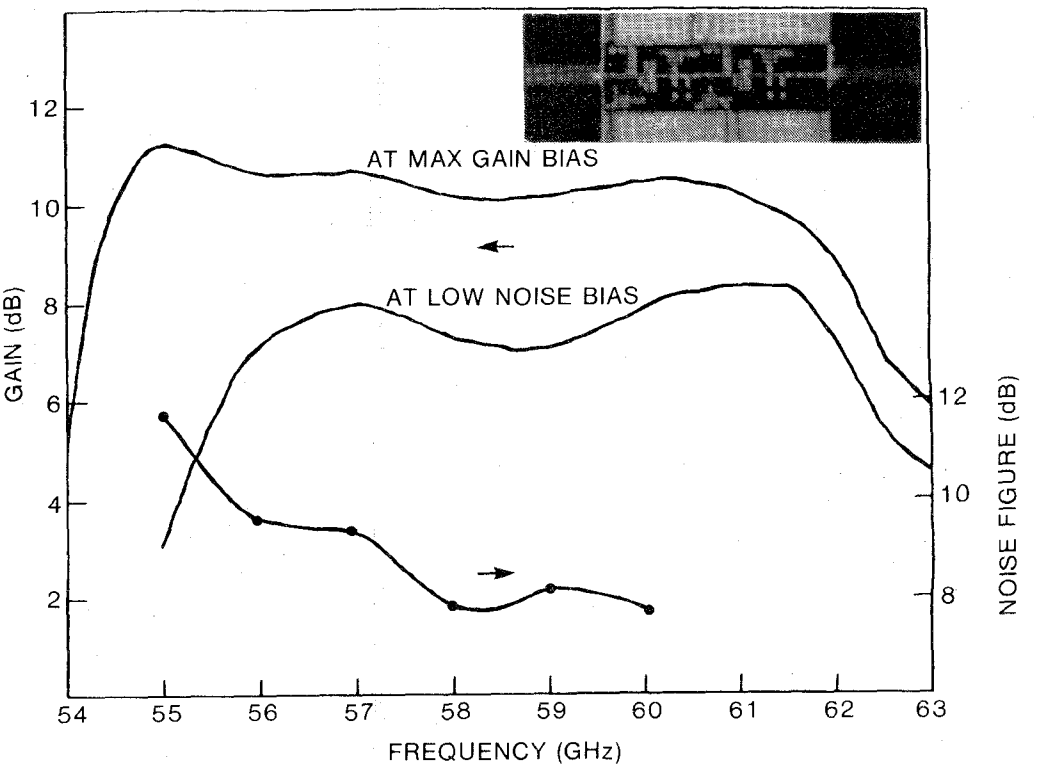


Fig. 14. Performance of a dual-stage MMIC LNA.

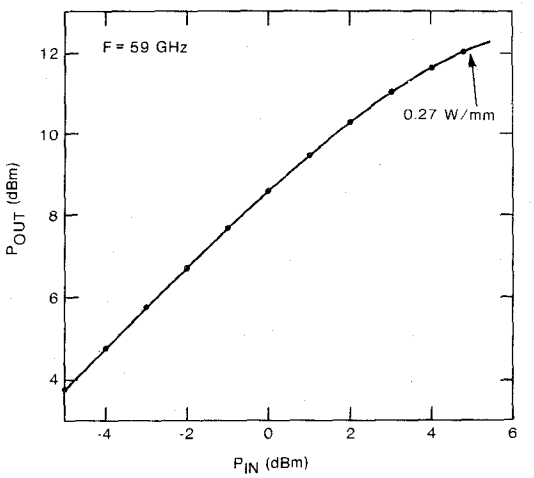


Fig. 15. P_{out} versus P_{in} of a dual-stage MMIC LNA.

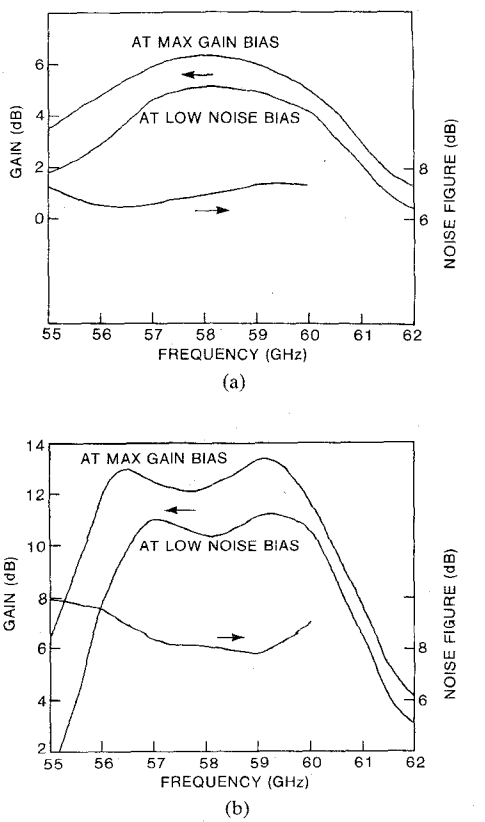


Fig. 16. Performance of (a) single- and (b) dual-stage LNA's from MBE wafers.

improvement in linear gain was observed in the dual-stage amplifier.

To achieve usable gain for system applications, MMIC modules were cascaded. Fig. 17 is a photograph of a six-stage LNA. The amplifier exhibited a minimum noise figure of 8.01 dB and an associated linear gain of 30 dB across the 56.2–60 GHz band, as illustrated in Fig. 18. Stable operation was obtained with this amplifier.

C. Power MMIC Amplifier Results

The performance of the power MMIC's from both VPE and MBE wafers was evaluated. Circuits from the VPE wafers with different MESFET device parameters such as gate length and channel height were studied. Devices from the MBE wafers were intended for 60 GHz operation and all had a 0.3 μm gate length. Since the MBE wafer had a p^- buffer layer between the active layer and the semi-insulating substrate, the carriers were well confined within

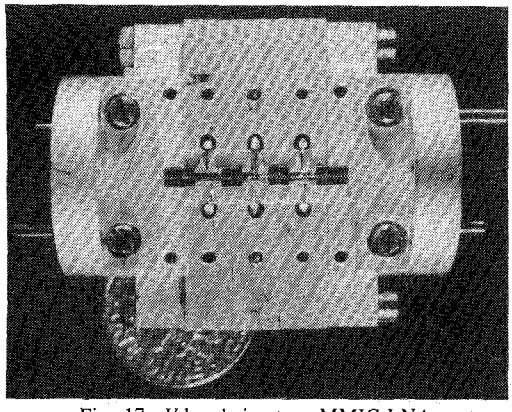


Fig. 17. *V*-band six-stage MMIC LNA.

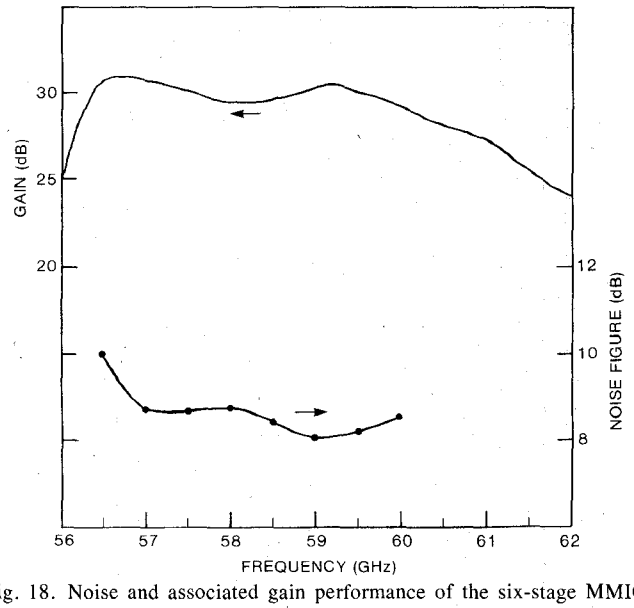


Fig. 18. Noise and associated gain performance of the six-stage MMIC LNA.

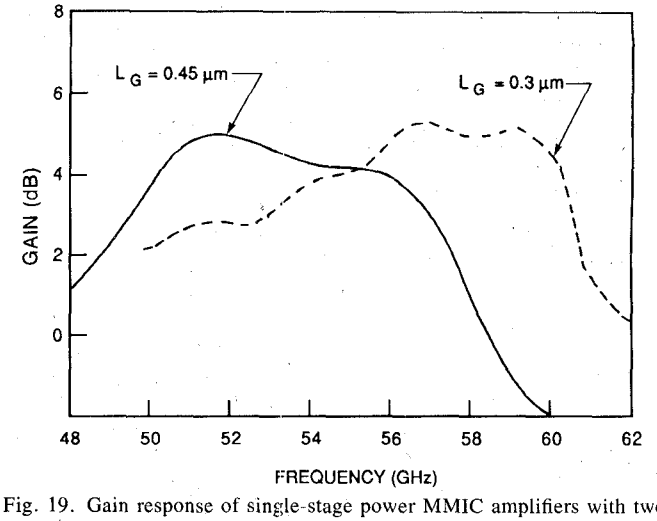


Fig. 19. Gain response of single-stage power MMIC amplifiers with two different device parameters from VPE wafers.

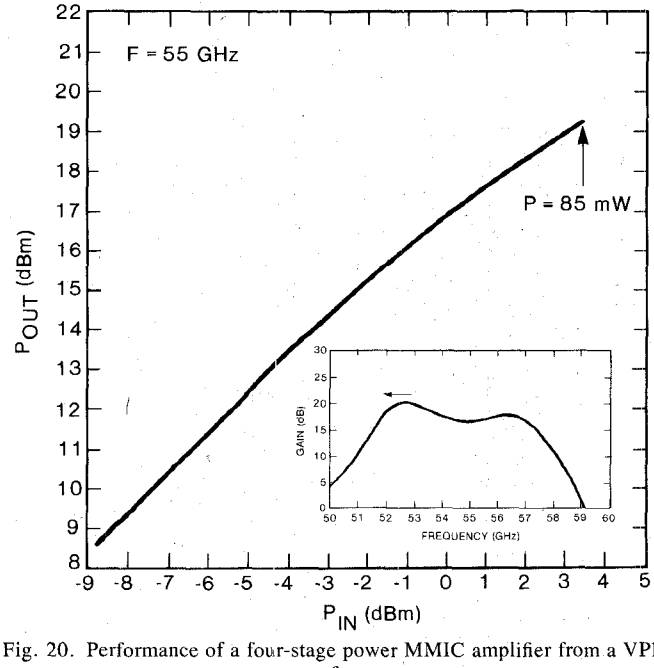


Fig. 20. Performance of a four-stage power MMIC amplifier from a VPE wafer.

the channel, resulting in low output conductance for the MESFET.

The measured small-signal gain of the MMIC PA's from the VPE wafer with the devices of longer gate length (0.42 μm) was greater than 4 dB from 50 to 56 GHz, as shown in Fig. 19. For comparison, the performance of MMIC's with shorter gate length (0.3 μm) VPE MESFET's is plotted in the figure. As expected, the frequency band was shifted, resulting in signal amplification above 60 GHz. No degradation in millimeter-wave performance was observed.

MMIC modules were cascaded to achieve higher power gain, and stable operation was observed. Fig. 20 shows the performance of a four-stage amplifier with longer gate length VPE MESFET's. Better than 17 dB of power gain was measured in the 52–57 GHz frequency range. At 55 GHz, 85 mW of output power was obtained, with an associated gain of 15.8 dB.

Fig. 21 shows the measured results for the MMIC amplifiers from MBE wafers. Linear power gain of better than 4.5 dB was obtained from 57 to 60.5 GHz. At 58 GHz, an output power of 95 mW, and an associated power-added efficiency and gain of 11 percent and 3.6 dB, respectively, were achieved. At the optimum efficiency bias, 15.3 percent power-added efficiency was obtained, with an associated output power and gain of 73 mW and 3 dB, respectively, measured at the same frequency. The corresponding drain efficiency was 31.3 percent.

To obtain higher output power, Wilkinson power divider and combiner circuits on 0.127-mm-thick fused-silica substrates were used to parallel two cascaded MMIC's. The use of external circuits reduced the use of the more expensive GaAs real estate and minimized total circuit RF loss. The circuit loss of a pair of the divider/combiner network was measured to be 1 dB in this frequency band. Fig. 22 is a photograph of the dual-stage balanced amplifier. The measured small-signal gain response was better than 7.5 dB from 56.5 to 61.5 GHz, as shown in Fig. 23.

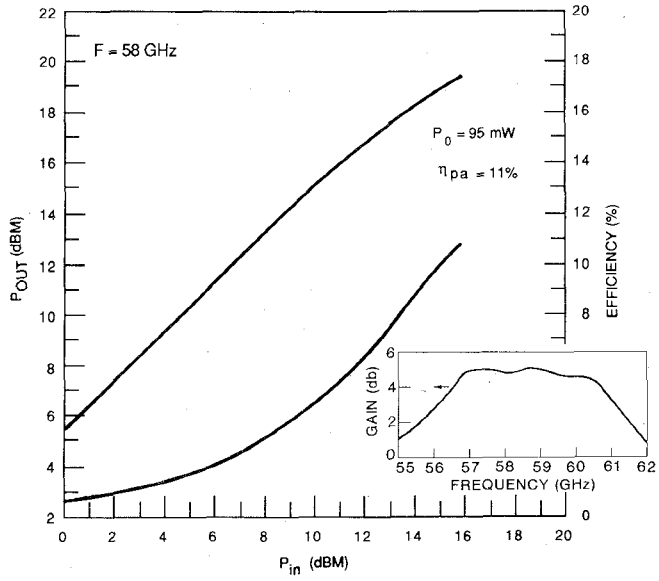


Fig. 21. Performance of a single-stage power MMIC amplifier from an MBE wafer.

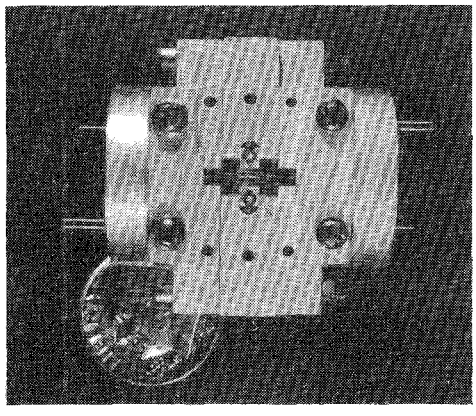


Fig. 22. *V*-band two-stage balanced MMIC power amplifier.

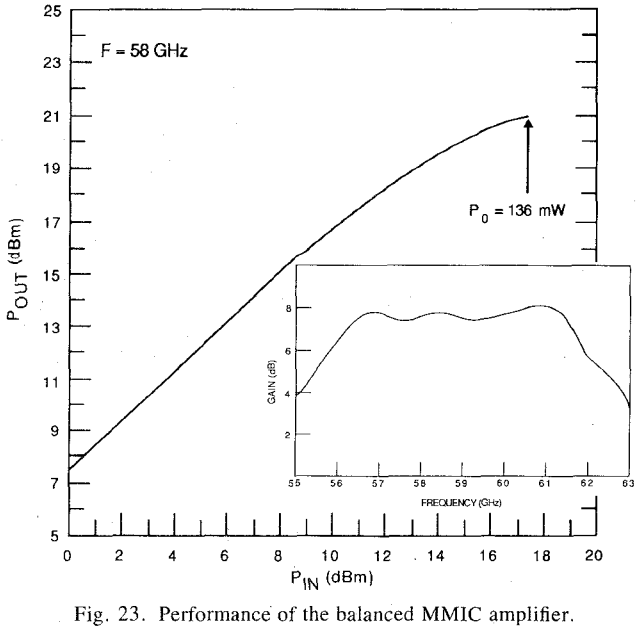


Fig. 23. Performance of the balanced MMIC amplifier.

Fig. 23 also presents the power transfer characteristics of the complete amplifier, including the power divider/combiner circuits. An output power of 136 mW was obtained at 58 GHz, with a corresponding gain of 4 dB.

VI. Conclusions

Monolithic circuits with built-in dc-blocking capacitors and bias networks have been developed at *V*-band. Excellent millimeter-wave performance has been demonstrated over a wide frequency band beyond 60 GHz. Single- and dual-stage LNA's using MESFET's were designed and fabricated. A noise figure as low as 6.5 dB from a single-stage LNA, and useful gain of 30 dB from a cascaded six-stage amplifier, were obtained. *V*-Band GaAs monolithic PA's using a 300 μm gate width MESFET have demonstrated a maximum power-added efficiency of 15.3 percent from a single-stage PA and an output power of 136 mW from a balanced amplifier at 58 GHz. Device/circuit modeling has also resulted in stable multistage amplifiers, providing power gain exceeding 17 dB. These results represent state-of-the-art performance from MMIC's in these frequency bands. This work demonstrates the potential for using MESFET MMIC technology in the low-noise and power areas for future millimeter-wave system applications such as satellite communications and electronic warfare.

Acknowledgment

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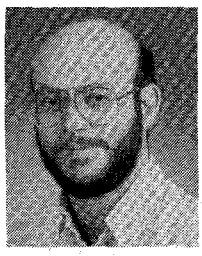

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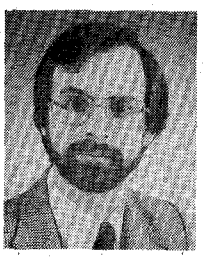

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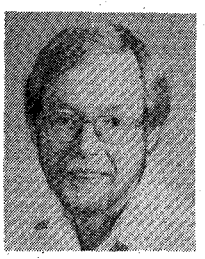

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